REMARKS

Claims 1-40 were originally filed in the application. Claims 6-36 and 38-40 were withdrawn from consideration as being drawn to a non-elected invention, claims 9 and 10 were canceled and claims 41 and 42 were added to the elected invention. The foregoing leaves claims 1-8 and 11-42 remaining in the application, of which claims 1-5, 37, 41 and 42 are drawn to the elected group I.

By this amendment, the claims have been significantly revised to define the invention more clearly and with greater particularity. Applicant believes the claims as amended avoid any possible reasonable interpretation that they would be rendered obvious by any combination of the cited references.

Applicant expresses continued objection to the restriction requirement in this application, which Applicant is unable to comprehend. The claims are parent and dependent claims, and the Examiner has not pointed out which claims are regarded as a subcombination and which as the combination. In fact, there are no separate subcombination claims, there are only independent and dependent claims. The Examiner requests Applicant to show why the restriction requirement is improper. Applicant refers to §806.05(c) of the MPEP, example one, which states: "Where a combination as claimed does not set forth the details of the subcombination as separately claimed, the inventions are distinct and restriction is proper if reasons exist for insisting upon the restriction." Here the alleged subcombinations are not "separately claimed," since they depend from a parent claim drawn to the combination. More generally stated, it is Applicant's position that an independent claim and a dependent claim (depending from the independent claim) are not properly subject to a restriction

requirement. The Examiner has not cited any support for a position to the contrary. Applicant respectfully requests that the restriction requirement be withdrawn.

Further, claims 6-18 and 38 were stated to be classed in class 59, subclass 237. Class 59 relates to manufacture of chains. This application has nothing to do with chain making. The remaining group classifications are also somewhat implausible, since class 257 subclass 83 dealing with active solid state devices, subclass 83 specifying an incoherent light source. The claims specified for that group have nothing to do with coherent or incoherent light. At best the claims deal with any kind of optic communication, not structure for a solid state light generator. Class 257 subclass 777 (group IV) deals with active solid state devices (as in group I) but the subclass deals with chips mounted on a chip. This is not the subject matter of invention specified by the claims listed in group IV. Lastly class 359 subclass 118 (group III) deals with optics, and the subclass deals with optical local area networks. Applicant submits that the subject matter of the claimed inventions is a hybrid, a solid state device (as in class 257/777) that includes semiconductors formed on a wafer and optical communications between wafers. Accordingly, if the Examiner insists on a restriction requirement, the particular grouping should, Applicant submits, be revised.

Claims 1-5 and 37 were rejected under 35 U.S.C. §103(a) as unpatentable over Zavracky et al. in view of Fitch et al. and Van Zeghbroeck. This rejection is respectfully traversed.

The rejection states that Zavracky shows a three-dimensional mutli-layer microprocessor structure with silicon on insulator structures, referring to FIG. 14, and col. 5, line 34, and shows the use of fiber optic interconnects, referring to col. 12, line

39. This characterization of Zavracky is incorrect. The Zavracky patent does not show the use of fiber optic interconnects and Applicant is unable to find any such showing. Line 34 of column 5 refers only to a light-emitting diode array.

As shown in FIG. 14 of the reference, the light-emitting diode array 830 is on the uppermost layer and forms an illuminated display. For example, the light-emitting diodes in the array may be selectively driven by the drivers 834 and 832 to display the letter "A," or anything else. However, this is not a "fiber optic interconnect."

At lines 48 and 49 of column 5 in Zavracky, there is a statement that the LED elements or arrays "*can be used along with fiber optics to optically interconnect different layers of the structure.*" The foregoing is a general suggestion or idea to optically interconnect different layers of the structure, but does not contain the requisite teaching or showing as to how to accomplish that suggestion in the combination of Zavracky.

This statement in Zavracky is in the nature of an afterthought of no value or utility. Clearly, if Zavracky had thought such a more useful structure than the electrical vias that are used, he would have invented and disclosed such an optical system. The Examiner appears to recognize this insufficiency by making reference to the patent to Van Zeghbroeck.

The Examiner is respectfully requested to reconsider the Zavracky patent should it persist in rejecting claim 1, and point out the fiber optic structure and interconnections made therewith that the rejection asserts is present in Zavracky.

The Examiner applies the Van Zeghbroeck patent to show the "details" of a fiber optic coupling "which specifically shows a perpendicular fiber mounting" and that "it

would have been obvious to use the Van Zeghbroeck technique in the Zavracky et al. device to provide details which are not here described."

The Van Zeghbroeck patent discloses a system for bidirectional full duplex optical communication between two spaced physical locations. The Van Zeghbroeck system can be used "over relatively short distances, including optical interconnection of computer components and/or systems" (col. 4, lines 3-8). The patent describes a unique semiconductor device that defines a photo-diode 21 and a light-emitting diode (LED) 20 in a stacked relationship. This device is positioned underlying an electrode 38 containing a window 39 that defines a light transmissive window. The photo-diode and LED of the semiconductor devices are controlled in conjunction with respective electronic circuits containing differential amplifiers, the details and operation of which are set forth in the patent. By using a pair of those semiconductor devices and incorporating an optical fiber 10 between the two devices, bi-directional full duplex optical transmission of light pulses is accomplished. In each such semiconductor device, an end of optical fiber 10 is positioned adjacent the window 39 to receive light issued by the LED 20 through window 39 for propagation along the optical fiber, and also to transmit light propagating through the optical fiber 10 originating at the second semiconductor device located at the remote end of the optical fiber. As illustrated, the axis of the optical fiber appears to be normal to the planar surfaces of the semiconductor material forming the semiconductor device. However, light going to and/or coming from the optical fiber propagates parallel to the optical fiber axis.

Although Zavracky contains the general statement of replacing the vias in his multi-layer processor structure with respective optical transmission devices, and Van

Zeghbroeck contains the statement that his bidirectional full-duplex optical transmission system may be incorporated within a processor, it is not apparent how this modification of Zavracky may be accomplished without additional invention.

No matter which combination of the foregoing references is constructed, none appears capable of assembly and/or disassembly by physical insertion or withdrawal, respectively, of the optical data bus. None is capable of coupling multiple nodes to different spaced locations along the length of an optical fiber; and none has light coupled to and from the side of the optical fiber.

Additionally, even if one were able to so combine the structures of the applied references, such a reconstruction would not anticipate or render obvious the invention defined by independent claims 1 and 37. As amended, claims 1 and 37 each specify that the optical coupling at the node is through the side of the optical data bus. Dependent claim 2, depending from claim 1, now specifies the couplers that are included in the optical data bus and recites that those couplings are at spaced locations along the bus. Claims 3 and 4, depending from claim 2, prescribe additional limitations.

Newly added dependent claim 41, further restricts the subject of claim 3, and newly added claim 42 depends from claim 41. Those new dependent claims are also believed to define allowable subject matter for the foregoing reasons.

Applicant's invention provides for optical data communication between a wafer (containing semiconductor circuits and optical nodes) and multiple external devices, of which may comprise additional wafers (also containing semiconductor circuits and optical nodes), with a single optical data bus, by coupling the optical data to and receiving data from the side of the optical data bus. The invention provides for a more

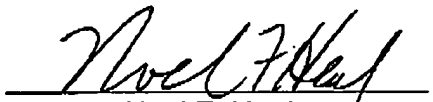
compact high speed system assembly that takes advantage of the benefit of optical communications and provides for easy disassembly and reassembly for repair.

Claims 9 and 10 have been cancelled without prejudice.

It is believed that the foregoing amendment to the specification and claims places the application in condition for allowance. Accordingly, an early notice of allowance is respectfully solicited.

Respectfully submitted,

Date: July 3, 2002



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ATTACHMENT FOR SPECIFICATION AMENDMENTS
VERSION WITH MARKINGS TO SHOW CHANGES MADE
U.S. Serial No. 09,618,708; Filed: July 18, 2000

The paragraph on page 7, beginning at line 5, was amended as follows:

In an alternate embodiment of the present invention, an integrated circuit device is provided that includes a plurality of adjacently stacked wafers, each wafer having a first surface, a second surface opposite the first surface and an optical transmission interface extending from the first surface through to the second surface, a semiconductor layer disposed on each first wafer surface, and a plurality of integrated circuits formed on each semiconductor layer. The plurality of integrated circuits include a node formed on the semiconductor layer adjacent to the optical transmission interface to couple optical data into and out of the plurality of integrated circuits. An optical data bus is included for coupling optical data between one wafer node and other nodes of wafers within the stack. The optical data bus extends axially through each of the optical transmission interfaces normal to each first wafer surface at each node. Alternatively, the foregoing type of optical transmission interfaces may be omitted and the nodes formed at an edge of each wafer such that the optical data bus extends along the edge of each wafer normal to each of the first wafer surfaces to form different interfaces therebetween. The integrated circuit device also includes the capability to replace defective wafers found in the stack of wafers.

The paragraph on page 6, beginning at line 2, was amended as follows:

The preceding and other shortcomings of the prior art are addressed and overcome by the present invention that provides an integrated circuit device. The device includes a wafer having a first surface, a second surface opposite the first

surface, an optical transmission interface extending from the first wafer surface through to the second wafer surface, a semiconductor layer disposed on the first wafer surface, and a plurality of integrated circuits formed on the semiconductor layer. An optical data bus extends through the optical transmission interface normal to the first wafer surface and a plurality of devices are coupled to the optical data bus. To provide optical coupling between the plurality of integrated circuits and the optical data bus, a node is formed on the semiconductor layer adjacent to the optical transmission interface. Alternatively, the foregoing optical transmission interfaces may be omitted and the node formed at an edge of the wafer such that the optical data bus is extended along the edge of the wafer normal to the first wafer surface, defining a different optical interface.

The paragraph on page 9, beginning at line 22, was amended as follows.

Referring to FIGs. 2a and 2b, to provide interconnectivity between the wafer circuitry 16 and external devices (not shown), each wafer node 18 includes a transmitter circuit 28 and a receiver circuit 30. For purposes of the present invention a single node 18 (transmitter/receiver circuit pair) or multiple nodes may be formed on the wafer 12. In the single node embodiment, a single optical data bus 20 or waveguide 22 (described below) extends at the node 18 through an optical transmission interface 26 to facilitate a single-channel broadcast architecture between the wafer 12 and external devices. Alternatively, the nodes 18 can be placed on the edge of the wafer 12[, thereby alleviating the need for the optical interfaces 26].

Application No. 09/618,708 TRW Docket No. 36-0032

ATTACHMENT FOR CLAIM AMENDMENTS
VERSION WITH MARKINGS TO SHOW CHANGES MADE
U.S. Serial No. 09,618,708; Filed: July 18, 2000

1. (Amended) An integrated circuit device comprising:

a wafer having a first surface, a second surface opposite said first surface and an optical transmission interface extending from said first wafer surface through to said second wafer surface;

a semiconductor layer disposed on said first wafer surface;

a plurality of integrated circuits formed on said semiconductor layer;

an optical data bus extending through said optical transmission interface normal to said first wafer surface, said optical data bus having first and second ends and being greater in length than the distance between the top of said semiconductor layer and said second surface, said optical data bus extending beyond both said semiconductor layer and said second surface with said first and second ends being positioned spaced from said semiconductor layer and from said second surface;

[a plurality of external devices] at least one device optically coupled to said optical data bus, said at least one device being external to and spaced from said wafer; and

a node formed on said semiconductor layer adjacent to said optical transmission interface and a side of said optical data bus, said node having means for optically coupling said plurality of integrated circuits and said optical data bus through said side of said optical data bus for providing optical data communication with said at least one device .

2. (Amended) An integrated circuit device as recited in claim 1, wherein said [wafer is formed of a thermally conductive material] optical data bus includes a plurality of couplers longitudinally spaced apart along said optical data bus, each of said couplers for translating incident optical energy propagating thereto in a direction normal to said optical data bus to optical energy propagating in opposite directions along the axis of said optical data bus and for translating the direction of propagation of a portion of incident optical energy propagating along said axis of said optical data bus to optical energy propagating in a direction normal to said axis and out said side of said optical data bus;

one of said plurality of couplers being positioned in alignment with said node on said wafer; and

at least one other of said plurality of couplers being optically coupled to said at least one device.

3. (Amended) An integrated circuit device as recited in claim [1] 2, wherein each of said [wafer is formed of a material selected from the group consisting of diamond and sapphire] couplers comprise a Bragg diffraction grating.

4. (Amended) An integrated circuit device as recited in claim [1] 2, wherein said [semiconductor layer is formed of a material selected from the group consisting of silicon (Si), germanium (Ge) gallium arsenide (GaAs), gallium phosphide (GaP), indium phosphide (InP), and indium arsenide (InAs)] at least one device comprises a plurality of devices, each of said devices being spaced from one another along said optical data bus, and wherein each of said plurality of said couplers of said optical data bus are positioned adjacent a respective one of said plurality of devices.

5. (Amended) An integrated circuit device as recited in claim [1] 2, wherein [each said integrated circuit is an application specific integrated circuit (ASIC)] said optical data bus comprises a slab of light transmissive dielectric material, said slab having a straight elongate geometry.

37. (Amended) An integrated circuit device comprising:

a wafer having a first surface, and a second surface opposite said first surface;

a semiconductor layer disposed on said first wafer surface;

a plurality of integrated circuits formed on said semiconductor layer;

an optical data bus extending along an edge of said wafer normal to said first wafer surface, and extending beyond both said semiconductor layer and said second surface, said optical data bus having first and second ends and a side and being greater in length that the distance between the top of said semiconductor layer and said second surface;

said optical data bus being physically disconnected from said optical transmission interface and said wafer;

a plurality of external devices coupled to said optical data bus; and

a node formed on said semiconductor layer adjacent to said wafer edge and a side of said optical data bus, said node [having] including means for optically coupling said plurality of integrated circuits and said optical data bus;

said optical data bus including a plurality of couplers longitudinally spaced apart along said optical data bus, each of said couplers for translating incident optical energy propagating thereto in a direction normal to said optical data bus to optical energy propagating in opposite directions along the axis of said optical data bus and for

translating the direction of propagation of a portion of optical energy propagating along said axis of said optical data bus incident thereon to optical energy propagating in a direction normal to said axis out a side of said optical data bus;

one of said plurality of couplers being positioned in alignment with said node; and

the remainder of said plurality of couplers being optically coupled to respective ones of said plurality of external devices.